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**UNITED STATES DISTRICT COURT**  
**NORTHERN DISTRICT OF CALIFORNIA**  
**SAN FRANCISCO DIVISION**

3COM CORPORATION,  
  
Plaintiff,

v.

D-LINK SYSTEMS, INC.

and

REALTEK SEMICONDUCTOR CORP.,  
  
Defendants.

Case No. CV-03-2177-VRW ENE

**REALTEK'S NOTICE OF MOTION AND  
MOTION FOR SUMMARY JUDGMENT  
OF INVALIDITY OF U.S. PATENT NO.  
5,307,459**

Judge: Vaughn R. Walker  
Date: December 20, 2007  
Time: 2:30 p.m.  
Courtroom: 6, 17th Floor

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**NOTICE OF MOTION AND MOTION**

TO PLAINTIFF AND ITS ATTORNEYS OF RECORD:

PLEASE TAKE NOTICE that on December 20, 2007 at 2:30 p.m. in Courtroom 6 of this Court located at 450 Golden Gate Avenue, San Francisco, California, or as soon thereafter as the matter may be heard, Defendant Realtek Semiconductor Corporation (“Realtek”) will and hereby does move this Court, pursuant to Rule 56 of the Federal Rules of Civil Procedure, for summary judgment that claim 1 of United States Patent No. 5,307,459 (“the ‘459 Patent”) is invalid. As grounds for its motion, as set forth fully in the accompanying Memorandum of Points and Authorities, Realtek states that, if claim 1 is construed as asserted by 3Com, the inventors named on the ‘459 patent were not the first to invent the claimed subject matter and the invention was on-sale in the United States more than one year before the application for the ‘459 patent was filed, rendering the claim invalid under 35 U.S.C. §§ 102(b) and (g).

This motion is based upon this Notice of Motion and Memorandum of Points and Authorities, the supporting declarations of Farzin Firoozmand (“Firoozmand Decl.”) and S.H. Michael Kim (“Kim Decl.”), the other papers and pleadings on file herein and on such other argument and evidence as may be presented to the Court at or prior to the hearing on this motion.

**MEMORANDUM OF POINTS AND AUTHORITIES**

**I. INTRODUCTION**

3Com accuses Realtek’s network interface controller chips of infringing claim 1 of the ‘459 patent. As discussed in Realtek’s Motion for Summary Judgment of Noninfringement of that patent, which is filed concurrently herewith, 3Com has no basis for that allegation. 3Com can not identify any Realtek product that “generates an indication signal to the host processor” as required by that claim. In particular, 3Com’s infringement position is premised on its belief that the “indication signal” need not actually be sent to the host processor in advance of a subsequent interrupt. That position ignores the plain import of the claim language requiring the “indication signal” to be “generated . . . to the host processor” Because there is no dispute that the alleged “indication signal” in the Realtek products is not “generated to the host” Realtek does not infringe this claim.

1 Realtek brings this motion in the alternative, to demonstrate that if the indication signal need  
 2 not be sent to the host to satisfy the requirements of claim 1, that claim is invalid. The subject matter  
 3 of claim 1, if so construed, was first invented by Farzin Firoozmand at Advanced Micro Devices Corp.  
 4 well before the alleged invention of the '459 patent. It was described in at least two issued patents that  
 5 are prior art to the '459 patent. That invention was also embodied in AMD's SUPERNET 2 Chip Set  
 6 product, which was publicly disclosed and placed on sale more than one year before the application for  
 7 the '459 patent was filed. Therefore, if construed as 3Com suggests, claim 1 of the '459 patent is  
 8 invalid.

## 9 **II. STATEMENT OF FACTS**

### 10 **A. The '459 Patent**

11 In this action plaintiff 3Com Corporation ("3Com") alleges that claim 1 of the '459 patent is  
 12 infringed by Realtek products. The '459 patent issued on April 26, 1994 from an application that was  
 13 filed on July 28, 1992. Kim Decl., Ex. A. The '459 patent discloses and claims an alleged  
 14 improvement to a network interface card, or NIC. NICs are used to transfer data to or from a host  
 15 computer over a network. *Id.* at 1:15-25. Data is generally transferred in "packets" or "frames" which  
 16 are groups of bytes consisting of the user data to be transferred and headers and footers describing the  
 17 data, its destination and the like.

18 NICs move data in both directions. That is, they both transmit data from the host over the  
 19 network, and receive data from the network destined for the host. In either event, data is first moved  
 20 into a temporary storage location in the NIC prior to its transmission over the network or its transfer to  
 21 the host. Once a data frame is received from the network into the buffer memory, the NIC will issue an  
 22 "interrupt" signal to the host computer telling the host that the data is available. The host processor  
 23 must then stop what it is doing, save its current environment so that it can resume the interrupted  
 24 function, and then deal with the data transfer request. The time spent preparing to service the interrupt  
 25 is called "interrupt latency" and can decrease the speed at which data can be transferred through the  
 26 NIC.

1 The '459 patent seeks to reduce that latency and increase data throughput by informing the  
 2 processor of the coming interrupt prior to receipt of all of the data frame in the NIC. Claim 1 of the  
 3 '459 patent reads:

4 1. An apparatus for transferring a data frame between a network  
 5 transceiver, coupled with a network, and a host system which includes a  
 6 host processor and host memory, the apparatus generating an indication  
 7 signal to the host processor responsive to the transfer of the data frame,  
 with the host processor responding to the indication signal after a period of  
 time, comprising:

8 a buffer memory for storing the data frame;

9 network interface logic for transferring the data frame between the host  
 system and the buffer memory;

10 host interface logic for transferring the data frame between the host system  
 11 and the buffer memory;

12 threshold logic for allowing the period of time for the host processor to  
 13 respond to the indication signal to occur during the transferring of the  
 data frame, wherein the threshold logic includes,

14 a counter, coupled to the buffer memory, for counting the amount of  
 data transferred to or from the buffer memory;

15 an alterable storage location containing a threshold value; and

16 means for comparing the counter to the threshold value in the alterable  
 17 storage location and generating an indication signal to the host  
 processor responsive to a comparison of the counter and the alterable  
 storage location.

18  
 19 Kim Decl., Ex. A at 42:42-68.

## 20 **B. The Firoozmand Patents**

21 On May 29, 1990 Farzin Firoozmand filed several patent applications relating to NICs.  
 22 Firoozmand Decl., ¶ 9. Two patents of particular interest here issued from those applications: U.S.  
 23 Patent 5,210,749 ("the '749 patent" or "Firoozmand I") and U.S. Patent 5,488,724 ("the '724 patent"  
 24 or "Firoozmand II"). *Id.*, Exs. 2 and 3. Mr. Firoozmand was an engineer with Advanced Micro  
 25 Devices Corp. ("AMD") between 1985 and 1989. *Id.*, ¶ 8. He was responsible for the project that led  
 26 to AMD's commercial introduction of its Supernet II NIC product. *Id.* Mr. Firoozmand provided an  
 27  
 28

1 invention disclosure statement to AMD's patent counsel on May 15, 1989, which began the process of  
2 applying for those patents. *Id.*, ¶ 11.

3 Like the asserted '459 patent, Mr. Firoozmand's NIC included a buffer memory for storing data  
4 temporarily as it was received from or transferred to the network. *Id.*, ¶ 11. Like the '459 patent, Mr.  
5 Firoozmand's patents disclose a NIC that will initiate the transfer of data out of the buffer memory  
6 before an entire frame is received. *Id.*, ¶ 12. Like the '459 patent, Mr. Firoozmand's patents disclose  
7 that an adjustable threshold value that will determine how much data will be received into the buffer  
8 before the host is notified. *Id.*, ¶ 13.

### 9 C. The Commercial AMD SUPERNET II Products

10 The NIC circuitry disclosed in the Firoozmand I and II patents was implemented in a  
11 commercial product by AMD called the SUPERNET 2 chipset. Firoozmand Decl., ¶ 14. As disclosed  
12 in the AMD Data Sheets published in 1991, the SUPERNET 2 chipset consisted of the FORMAC Plus  
13 controller chip, a physical layer controller and physical data transmit/receiver chips. *Id.*, Ex. 8 at  
14 RT008839. Just as described in the Firoozmand I and II patents, the FORMAC Plus chip includes a  
15 buffer memory, a counter to determine the amount of data transferred to the buffer memory, and an  
16 alterable storage location to store a threshold value. *Id.*, ¶ 17-18. In operation, the count of data  
17 received by the buffer is compared to the threshold value stored in the register and, when a threshold  
18 amount of data has been received, the RDATA indication signal is generated to the host. *Id.*, ¶ 17. In  
19 response to the RDATA signal, the host requests access to the buffer memory and reads the frame data.  
20 Thus, the host can begin to receive data from the buffer while the buffer is uploading data from the  
21 network. *Id.*, ¶ 20.

22 The SUPERNET 2 chipset was offered for sale in February 1991. That month's issue of LAN:  
23 Local Area Network Magazine reported AMD's announcement of the commercial availability of the  
24 SUPERNET 2 chipset, including the FORMAC Plus chip. Firoozmand Decl., Ex. 7. That article states  
25 that AMD is offering the SUPERNET 2 for sale at a price of \$225.00 in lots of one thousand.

### 1 **III. ARGUMENT**

#### 2 **A. Legal Standard**

3 Summary judgment may be appropriate when no genuine dispute of material fact exists. *Irdeto*  
 4 *Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1299 (Fed. Cir. 2004), quoting *Bai v. L & L*  
 5 *Wings, Inc.*, 160 F.3d 1350, 1353 (Fed. Cir. 1998). Once one party moves for summary judgment and  
 6 supports its motion with admissible evidence, the non-moving party must set forth specific facts  
 7 showing that there is a genuine issue for trial. Fed. R. Civ. P. 56(e). “A nonmovant must do more than  
 8 merely raise some doubt as to the existence of a fact” and must set forth enough evidence to enable a  
 9 jury to reasonably find for the nonmoving party. *Avia Group Int’l, Inc. v. L.A. Gear California, Inc.*,  
 10 853 F.2d 1557, 1560 (Fed. Cir. 1988); *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 249-50 (1986).  
 11 When the nonmoving party fails to make a showing sufficient to establish evidence of an element  
 12 essential to its case, the complete failure of proof concerning the essential element necessarily renders  
 13 all other facts immaterial and a summary judgment is warranted. *Rotec Indus., Inc. v. Mitsubishi*  
 14 *Corp.*, 215 F.3d 1246, 1250 (Fed. Cir. 2000). Summary judgment is as appropriate in a patent case as  
 15 it is in any other case.” *C.R. Bard Inc. v. Advanced Cardiovascular Sys., Inc.*, 911 F.2d 670, 672 (Fed.  
 16 Cir. 1990); *see also Desper Prods., Inc. v. Qsound Labs, Inc.*, 157 F.3d 1325, 1332 (Fed. Cir. 1998).

17 A patent is not valid if the alleged invention claimed is not novel, or it would have been  
 18 obvious to one of ordinary skill in the art. 35 U.S.C. §§ 101-103. A lack of novelty can be shown  
 19 where the claim is anticipated, that is when it is disclosed in a patent filed or a printed publication  
 20 dated before the alleged invention, *id.* § 102(a), or if the invention was publicly known or on sale more  
 21 than one year before the patent application was filed. *Id.*, § 102 (b). Finally, a patent claim is invalid if  
 22 it was first invented in the U.S. by someone other than the patentee who did not abandon, suppress or  
 23 conceal the invention. *Id.*, § 102(g). Anticipation requires a showing that a prior art reference  
 24 disclosed or included, either expressly or inherently, every element of the patent claim. *Celeritas*  
 25 *Techs., Ltd. v. Rockwell Int’l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998).

**B. The '459 Patent is Invalid in Light of Firoozmand**

1. Firoozmand Was First to Conceive and First to Reduce to Practice the Claimed Invention.

A patent claim is invalid if it was invented in this country first by someone other than the named inventor(s). 35 U.S.C. § 102(g). The inventions disclosed in the Firoozmand patents are prior art to 3Com's patents. Presumptively, the first-filed application is prior art to a later application. However, if the patentee on the later-filed patent claims to have invented before the earlier patent application, there is an issue of priority that must be resolved. 35 U.S.C. §102(g) controls such disputes over priority. That section holds that a patent is invalid if

before [the patentee's] invention thereof, the invention was made by another inventor who had not abandoned, suppressed or concealed it.

35 U.S.C. §102(g)(2).

The person who is first to reduce to practice is *prima facie* the first inventor. *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996). Mr. Firoozmand's invention was constructively reduced to practice on May 20, 1990 because filing a patent application is a constructive reduction to practice. *Hazeltine Corp. v. United States*, 820 F.2d 1190, 1196 (Fed. Cir. 1987). Firoozmand therefore reduced his invention to practice no later than the May 20, 1990 filing of his patent application. 3Com may claim to have conceived of the '459 invention before May 20, 1990. In order to prevail on that claim 3Com has the burden of coming forward with sufficient evidence to support its claimed date of conception. *C.R. Bard*, 79 F.3d at 1577. 3Com has not produced or pointed to any evidence to establish a date of conception before Mr. Firoozmand's. Because Mr. Firoozmand was the first to conceive and the first to reduce to practice, he is the first inventor under 35 U.S.C. §102(g).

Even if 3Com could somehow produce evidence to establish its date of conception before Mr. Firoozmand's, 3Com would then bear the burden of providing evidence to prove that its named inventors worked diligently to reduce the invention to practice. *C.R. Bard*, 79 F.3d at 1578. Such a showing requires proof that the inventors worked throughout the entire period from a date just prior to Firoozmand's reduction to practice until their own. *Monsanto Co. v. Mycogen Plant Science, Inc.*, 261 F.3d 1356, 1368-69 (Fed. Cir. 2001). 3Com cannot provide the required evidence to show either that it

1 was the first to invent or, even if so, that its inventors were diligent. As such, Mr. Firoozmand's prior  
 2 invention, as described in his patents, constitutes prior art to the '459 patent.

3 2. Firoozmand's Patents Disclose Every Element of Claim 1 of the '459 Patent

4 a) "a buffer memory for storing the data frame."

5 Firoozmand I discloses buffer memory 116 for temporary storage of data frames that are  
 6 transferred between a host system and the network. *See, e.g.*, Firoozmand Decl., Ex. 2 at 8:42-45; 9:8-  
 7 14; Fig. 4. Firoozmand II likewise discloses the required buffer memory. *See, e.g., id.*, Ex. 3 at Fig 4;  
 8 and corresponding text, 17:23-36.

9 b) "Network Interface logic for transferring the data frame between the  
 10 network transceiver and the buffer memory"

11 Firoozmand I and II disclose the FORMAC PLUS Medium Access Controller 20 including  
 12 logic that transfers data frames between buffer 126 and the network. "The Medium Access Controller  
 13 120 implements proper network access protocol, receiving and transmitting frames of data..."  
 14 Firoozmand Decl., Ex. 2 at 8:48-50. Furthermore, "[t]he medium access controller 120... is interfaced  
 15 to buffer memory 126..." *Id.* at 8:58-60.

16 c) "threshold logic for allowing the period of time for the host processor to  
 17 respond to the indication signal to occur during the transferring of the  
 data frame, including"

18 Firoozmand I discloses the required threshold logic. In particular, logic in the MAC controller  
 19 instructs the DMA controller 124 to indicate the availability of a data frame when a threshold amount  
 20 of data is available. *See, e.g.*, Firoozmand Decl., Ex. 2 at 15:30-62. Firoozmand II makes the same  
 21 disclosure. *Id.*, Ex. 3 at 18:65 – 19:15. As will be detailed below, these patents disclose every element  
 22 required by the "threshold logic."

23 i. "a counter, coupled to the buffer memory, for counting the  
 24 amount of data transferred to or from the buffer memory"

25 Firoozmand I discloses such a counter to one skilled in the art. It states that the threshold logic  
 26 determines whether "the number of words [e.g. bytes] received in the buffer 126 received from the  
 27 network exceeds the value RTHR of the receive threshold." Firoozmand Decl., Ex. 2 at 15:58-60. In  
 28 order to have that number available, the system required a counter to count the bytes transferred into  
 the buffer memory. *Id.* Such counters were widely known and easily implemented by those skilled in

the art at the time, and one way of implementing such a counter using pointers is disclosed. *Id.* at 15:63-16:5. This disclosure is incorporated by reference and also present in Firoozmand II. *See id.*, Ex. 3 at 18:66-19:14.

ii. “an alterable storage location containing threshold value”

Firoozmand I discloses an alterable storage location, register 187, which contains a threshold value RTHR. Firoozmand Decl., Ex. 2 at 15:43-58. Firoozmand II incorporates that disclosure by reference. *Id.*, Ex. 3 at 19:11-14. As such, this claim element is disclosed and enabled. Firoozmand Decl., ¶ 12.

iii. “means for comparing...and generating an indication signal to the host processor responsive to a comparison of the counter and the alterable storage location.”

3Com is taking the position that the “indication signal” need not be sent to the host. *See* Realtek’s Motion for Summary Judgment of Non-Infringement of the ’459 Patent. In particular, 3Com is arguing that this claim limitation is met by Realtek products where the comparison circuitry generates a signal to the host interface logic, and the host interface logic then issues an interrupt to the host processor. *Id.* If that scope of claim construction were to be adopted, this claim element is disclosed in the Firoozmand I and II patents. In particular, Firoozmand I disclose a means for comparing the number of bytes received in buffer memory 126 to a threshold value RTHR. Firoozmand Decl., ¶ 12. If that comparison shows that a sufficient number of bytes have been received, the comparison means in controller 120 asserts RDATA signal to the host interface logic in DM, Firoozmand Decl., Ex. 2 at controller 124. *Id.*, ¶ 13. In response to the RDATA signal, DMA controller 124 issues an interrupt to the host indicating that data is available for transfer. *Id.* In this way the host system is allowed time to respond to the interrupt before the entire frame is received into buffer memory 116. Interrupt latency is therefore reduced. *Id.* To the extent that 3Com is correct in its position that a signal created by the comparing means and sent to the host interface logic, but not the host is an “indication signal,” the means for comparing claim limitations is disclosed in Firoozmand I and II. That correspondence is set out in more detail in claim charts prepared by Mr. Firoozmand. *Id.*, Exs. 5 and 6.

**B. The '459 Patent is Invalid In Light of the AMD Supernet 2 Chipset.**

The NIC circuitry described in the Firoozmand patents was implemented into AMD's SUPERNET 2 chipset. Firoozmand Decl., ¶ 14. AMD offered that chipset for sale more than one year before the application for the '459 patent was filed. As such, claim 1 of the '459 patent is invalid under 35 U.S.C. § 102(b). A patent claim is invalid under the on-sale bar of § 102(b) when the invention is both the subject of an offer to sell and it is either reduced to practice or is ready for patenting. *Pfaff v. Wells Electronics, Inc.*, 525 U.S. 55, 67 (1998). As will be shown below, the SUPERNET 2 chipset was clearly on-sale. Since that product included every element of claim 1 as asserted by 3Com, that claim is invalid.

**1. AMD Offered the SUPERNET 2 for Sale in February 1991.**

A patent is invalid under 35 U.S.C. § 102(b) if, more than one year before the patent application is filed, the invention was 1) offered for sale in the United States and 2) the invention was reduced to practice or ready for patenting. *Pfaff*, 525 U.S. at 67. The first prong requires a showing of a commercial offer for sale. *Allen Eng'g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1352 (Fed. Cir. 2002). Whether there has been an offer is determined under general principles of commercial law. *Id.* By February 1991 AMD publicly and widely announced the availability of the SUPERNET 2 chipset, including the price at which it would sell that product. Firoozmand Decl., Ex. 7, Kim Decl., Ex. 3. For example, the February 1991 issue of "LAN: Local Area Network Magazine" included an article entitled "AMD Introduces FDDI Chip for Half-Size Cards." That article describes the SUPERNET 2 chipset as including the FORMAC Plus media access controller chip, a physical layer controller chip and transmit and receive chips. *Id.* The article, which quotes AMD's FDDI product marketing manager Basil Alwan at length, states that AMD is offering the chipset at a price of \$225.00 in lots of one thousand, and that AMD anticipated that "commercial quantities" of the chips would be available by the end of March, 1991. *Id.* That same announcement was reported in June 1991 in AMD's own magazine sent to its customers. Kim Decl., Ex. 3 (AMD00574). Those published reports state the price as \$225.00 when ordered in quantities of one thousand. These announcements constitute offers to sell the SUPERNET 2 chipset, quoting price and quantity. As such, the first prong of the on-sale bar test is satisfied.

1 The next prong considers whether the item offered for sale is sufficiently definite that it could  
 2 be described in a patent application. *Pfaff*, 525 U.S. at 67. That prong is obviously met here as the  
 3 patent applications were filed well before the offers for sale.

4 2. The AMD SUPERNET 2 Included Every Element of Claim 1 of the '459 Patent.

5 There is also no dispute that the subject of AMD's offers to sell, the SUPERNET 2 chipset,  
 6 included every element of claim1 as it has been asserted by 3Com. That is shown by the patent  
 7 applications Mr. Firoozmand prepared describing the FORMAC Plus chip and associated circuitry. It  
 8 is also confirmed by the 1991 Data Sheets prepared by AMD describing that product. As will be  
 9 shown below, that Data Sheet confirms that the SUPERNET 2 chipset included every element of  
 10 claim1.

11 a) "a buffer memory for storing the data frame."

12 The AM79C830 "FORMAC Plus" chip included a buffer memory for storing data frames  
 13 communicated between the host and the network medium. Firoozmand Decl., ¶ 18, Ex. 8 at  
 14 RT008842; RT00884 (Fig. 4).

15 b) "network interface logic for transferring the data frame between the  
 16 network transceiver and the buffer memory"

17 The FORMAC Plus included logic that transfers data frames between the buffer and the  
 18 network. *Id.*, ¶ 18, Ex. 8 at RT008841 ("The receive demultiplexer in the FORMAC Plus formats four  
 19 bytes of data into a 32-bit long word which is temporarily stored in the receive FIFO until the buffer  
 20 memory is ready to receive it. The FORMAC Plus sets up addresses on the 16-bit address line to store  
 21 the frame in buffer memory.")

22 c) "threshold logic for allowing the period of time for the host processor to  
 23 respond to the indication signal to occur during the transferring of the  
 data frame, including:"

24 The FORMAC Plus controller includes threshold logic that informs the host that a frame is  
 25 available for transfer while frame data is still being received into the buffer. Firoozmand Decl., ¶ 19.  
 26 As will be detailed below, these SUPERNET 2 chipset included every element required by the  
 27 "threshold logic."

28 i. "a counter, coupled to the buffer memory, for counting the  
 amount of data transferred to or from the buffer memory"

1 The FORMAC Plus included counters coupled to the buffer memory for counting the amount  
 2 of data received by the buffer. In particular, buffer memory queue counters keep track of the number  
 3 of long (32-bit) words transferred into the buffer memory. *Id.*, ¶ 19, Ex. 8 at RT008880.

4 ii. “an alterable storage location containing threshold value”

5 The FORMAC plus included an alterable storage location containing a threshold value.  
 6 Firoozmand Decl., ¶ 19. A Frame Threshold Register FRMTHR held both the receive threshold value  
 7 RTHR and the transmit threshold value RTHR. *Id.*, Ex. 8 at RT009006. That register could be  
 8 changed. *Id.*

9 iii. “means for comparing...and generating an indication signal to  
 10 the host processor responsive to a comparison of the counter and  
 11 the alterable storage location.”

12 Using 3Com’s construction of this term, namely that the “indication signal” need not be sent to  
 13 the host, this claim limitation is present in the SUPERNET 2 product. *See* Realtek’s Motion for  
 14 Summary Judgment of Non-Infringement of the ’459 Patent. The SUPERNET 2 included circuitry  
 15 that compared the number of long words transferred to the buffer memory to the receive threshold  
 16 value RTHR. Firoozmand Decl., ¶ 20. If that comparison shows that a sufficient number of bytes have  
 17 been received, the comparison means asserts the RDATA signal to the host. *Id.* The host responds  
 18 with a HSREQ read request signal, and the host begins to read data out of the buffer before while  
 19 frame data is still being written into the buffer. *Id.* In this way the host system is allowed time to  
 20 respond to the interrupt before the entire frame is received into buffer memory 116. Interrupt latency is  
 21 therefore reduced. To the extent that 3Com is correct in its position that a signal created by the  
 22 comparing means and sent to the host interface logic, but not the host is an “indication signal,” the  
 23 means for comparing claim limitations is disclosed in the AMD SUPERNET 2 chipset. That  
 24 correspondence is set out in more detail in claim charts prepared by Mr. Firoozmand. *Id.*, Exs. 5 and  
 25 6.

1 **IV. CONCLUSION**

2 For the reasons explained above, the Court should grant Realtek's Motion for Summary  
3 Judgment that Claim 1 of U.S. Patent No. 5,307,459 is invalid.

4  
5 Dated: November 16, 2007

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